CLAIMS

What is claimed is:

1. A semiconductor package comprising:

a die having a plurality of layers of low-K dielectric material, the die having a top surface, a bottom surface, and a plurality of side surfaces, each surface having associated corner and edge regions;

a wire bonding packaging substrate having a plurality of electrical contacts, the packaging substrate being positioned under the die;

a plurality of interconnects electrically connecting the die to the plurality of electrical contacts;

a molding interface material applied to at least a portion of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die; and

a molding cap covering at least a portion of the die, packaging substrate, interconnects, and molding interface material.

2. A semiconductor package as recited in claim 1, wherein the molding interface material controls by applying compressive stress to the die, thereby strengthening the die against the at least one of tensile and shear stresses.

3. A semiconductor package as recited in claim 1, wherein the molding interface material is polyimide.

4. A semiconductor package as recited in claim 3, wherein the molding interface material is on at least a portion of the plurality of side surfaces of the die.

5. A semiconductor package as recited in claim 4, wherein the molding interface material is also on a corresponding adjacent portion of the packaging substrate such that the die is firmly attached to the packaging substrate.

6. A semiconductor package as recited in claim 1, wherein the molding interface material is applied in multiple non-contiguous regions to the top surface of the die.

7. A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is rectangular in shape.

8. A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is triangular in shape.

9. A semiconductor package as recited in claim 6, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns.

10. A semiconductor package as recited in claim 1, wherein the molding interface material is a contiguous region on the top surface of the die excluding corner regions.

11. A semiconductor package as recited in claim 10, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns.

12. A semiconductor package as recited in claim 10, wherein the molding interface material is a contiguous region on the top surface of the die excluding edge regions.

13. A semiconductor package as recited in claim 12, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns.

14. A semiconductor package as recited in claim 1, wherein the molding interface material has a coefficient of thermal expansion between 5 ppm and 40 ppm.

15. A semiconductor package as recited in claim 14, wherein the molding interface material is over a substantial portion of the die such that a stress buffer zone is established between the die and the molding cap.

16. A semiconductor package as recited in claim 1, wherein the plurality of layers includes extra low-K dielectric material.

17. A method of forming a semiconductor package comprising:

providing a die with a layer of low-K dielectric material, the die having a top surface, a bottom surface, and a plurality of side surfaces, each surface having associated corner and edge regions;

applying a molding interface material to at least a portion of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die;

coupling the bottom surface of die with a packaging substrate, the packaging substrate having a plurality of electrical contacts;

connecting a plurality of interconnects between the die and the plurality of electrical contacts; and

forming a molding cap that covers at least a portion of the die, packaging substrate, interconnects, and molding interface material.

18. A method of forming a semiconductor package as recited in claim 17, wherein the molding interface material controls by applying compressive stress to the die, thereby strengthening the die against the at least one of tensile and shear stresses.

19. A method of forming a semiconductor package as recited in claim 17, wherein the molding interface material is polyimide.

20. A method of forming a semiconductor package as recited in claim 19, wherein applying the molding interface material is on at least a portion of the plurality of side surfaces of the die.

21. A method of forming a semiconductor package as recited in claim 20, further comprising applying the molding interface material on a corresponding adjacent portion of the packaging substrate such that the die is firmly attached to the packaging substrate.

22. A method of forming a semiconductor package as recited in claim 17, wherein the molding interface material is applied in multiple non-contiguous regions to the top surface of the die.

23. A method of forming a semiconductor package as recited in claim 22, wherein at least one of the multiple non-contiguous regions is rectangular in shape.

24. A method of forming a semiconductor package as recited in claim 22, wherein at least one of the multiple non-contiguous regions is triangular in shape.

25. A method of forming a semiconductor package as recited in claim 22, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns.

26. A method of forming a semiconductor package as recited in claim 17, wherein the molding interface material is a contiguous region on the top surface of the die excluding corner regions.

27. A method of forming a semiconductor package as recited in claim 26, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns.

28. A method of forming a semiconductor package as recited in claim 26, wherein the molding interface material is a contiguous region on the top surface of the die excluding edge regions.

29. A method of forming a semiconductor package as recited in claim 28, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns.

30. A method of forming a semiconductor package as recited in claim 17, wherein the molding interface material has a coefficient of thermal expansion between 5 ppm and 40 ppm.

31. A method of forming a semiconductor package as recited in claim 30, wherein the molding interface material is over a substantial portion of the die such that a stress buffer zone is established between the die and the molding cap.

32. A method of forming a semiconductor package as recited in claim 17, wherein the plurality of layers includes extra low-K dielectric material.

33. A method of forming a semiconductor package as recited in claim 17, further comprising:

cycling the temperature of the semiconductor package from -55 °C to 125 °C to create internal stress within the semiconductor package, wherein the die is stably integrated within the semiconductor package such that the reliability of the die is not substantially impaired by the internal stress of the semiconductor package.

34. A method of forming a semiconductor package comprising:

applying a first molding interface material to a front surface of a semiconductor wafer;

singulating the wafer to form a die, the die having a layer of low-K dielectric material, a top surface that corresponds to the front surface of the semiconductor wafer, a bottom surface, and a plurality of side surfaces, each surface having associated corner and edge regions;

coupling the bottom surface of the die with a packaging substrate, the packaging substrate having a plurality of electrical contacts;

connecting a plurality of interconnects between the at least one die and the plurality of electrical contacts; and

forming a molding cap that covers at least a portion of the at least one die, packaging substrate, interconnects, and molding interface material.

35. A method of forming a semiconductor package as recited in claims 34, further comprising:

applying a second molding interface material to any of the surfaces of the die.

36. A method of forming a semiconductor package as recited in claims 35, wherein the first and second molding interface materials are configured to control at least one of tensile and shear stresses experienced by the die.